Logic Synthesis with Nanowire Crossbar: Reality Check and Standard Cell-based Integration

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Abstract

Nanowire crossbar is one of the most promising circuit solutions for nanoelectronics. We show nanowire crossbars do not scale well in terms of logic density and speed. We consequently propose a Crossbar Cell design based on judicious use of silicon nanowire crossbars with microscale pitches and small dimensions. The Crossbar Cell is compatible with the conventional MOSFET fabrication and standard cell-based integration. We evaluate logic circuits using Crossbar Cells and show that they can improve density by more than fourfold over the traditional MOSFET circuits with the same process technology, while achieving close performance and over threefold power reduction.

1. Introduction

Nanowire crossbars are considered one of the most promising circuit solutions for nanoelectronics [1]. While a few works have addressed their use for logic circuits [1-3], it is unclear how they would compare with their MOSFET counterparts in this regard.

In this work, we report a reality check on the use of nanowire crossbars, in particular, FET-based crossbars, for logic circuits. We employ both theoretical analysis and simulation based upon devices reported in the literature. We show that nanowire crossbars do not scale well. While the most apparent advantage of nanowire crossbars over conventional MOSFET is their ultra high density of crosspoint devices, we find that the utilization of crosspoint devices decreases when the crossbar becomes larger, leading to lower logic density. Indeed, the achievable complementary logic density in a crossbar is $O(n^{-1})$, where n is the number of nanowires in each of the orthogonal arrays and is referred to as *the dimension of the nanowire crossbar* in this work. Moreover, we find that the delay of a crossbar logic circuit is $O(n)$. Based on the reality check, we provide insights into how nanotechnologists can improve crossbars with new materials and new device designs. To the best of our knowledge, we provide the first theoretical analysis of nanowire crossbars for logic implementation, as compared with their MOSFET counterparts.

Motivated by our reality check, we design Crossbar Cells that employ lithographically defined crossbars of a small dimension or n, rather than crossbars of large dimensions and nanoscale pitches. The Crossbar Cell design can be readily fabricated with minimal change to the standard MOSFET process and can be incorporated into MOSFET-based IC through the standard cell integration. Our SPICE simulation shows Crossbar Cells enjoy great advantages in density and power, compared with their MOSFET counterparts. Using Berkeley SIS and MCNC91 benchmark suite, we find that Crossbar Cells simultaneously improve speed, power, and area of MOSFET-based ICs in performance optimization. In area optimization, they reduce area by fourfold with a slight speed overhead (10%), when applied judiciously in standard logic synthesis. Our Crossbar Cell design demonstrates that nanowire crossbars can be judiciously employed to benefit existing MOSFET-based circuit design.

The rest of the paper is organized as follows. We theoretically analyze nanowire crossbar circuits and compare them with MOSFET in Section 2. We present the Crossbar Cell design in Section 3 and conclude in Section 4.

2. Reality Check

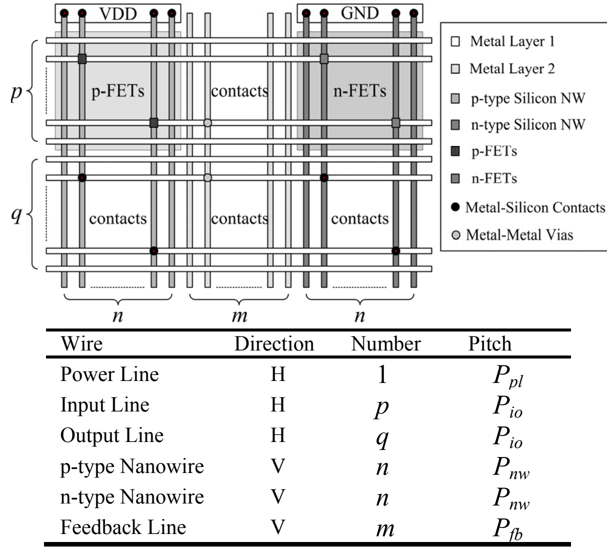
Crossbar arrays of various nanowires have been demonstrated[4, 5]. In a crossbar, the crossing of two nanowires forms a crosspoint, which may be independently configured to implement a FET (p-FET or n-FET) [6] or a diode [7]. While many have shown that nanowire crossbars compare favorably to their MOSFET counterparts for memory [5, 8], it is unclear how they would compare to their MOSFET counterparts in implementing logic, which is our focus.

We next analyze how logic circuits implemented in a complementary FET-based crossbar (See Fig 1), or *crossbar logic circuits*, will perform, especially in comparison with MOSFET logic circuits.

2.1 Area and Transistor Density

Ultra-high crosspoint density is the major advantage of nanowire crossbar. It has been shown to significantly increase the transistor density of crossbar memory circuits [5, 8]. However, we show that high crosspoint density does not translate into high transistor density for logic.

Theorem 1: *the density of transistors in a crossbar logic circuit is* $O(n^{-1})$.



Wire	Direction	Number	Pitch
Power Line	H	1	P_{pl}
Input Line	H	p	P_{io}
Output Line	H	q	P_{io}
p-type Nanowire	V	n	P_{nw}
n-type Nanowire	V	n	P_{nw}
Feedback Line	V	m	P_{fb}

Fig 1: A generic complementary FET-based crossbar and its geometric parameters.

Proof: Fig 1 illustrates a generic FET-based crossbar [3], which consists of a horizontal metal wire for VDD, a horizontal metal wire for GND, p horizontal metallic wires for inputs, q horizontal metallic wires for outputs, n n-type and n p-type semiconductive nanowires, and m vertical metallic wires for local interconnection. As mentioned above, the dimension of the crossbar is indicated by n.

Given these parameters, we can obtain area of the whole crossbar:

$$Area = X \times Y = (2n \times P_{nw} + m \times P_{fb}) \times (P_{pl} + (p+q) \times P_{io}) \,. \quad (1)$$

To minimize the area, we should set all the pitches as the minimal value, i.e., $P_{nw} = P_{io} = P_{pl} = P_{fb}$. Besides, because m, p, and q are relative to the dimension of the crossbar n, we assume $m = k_m \times n$, $p = k_p \times n$, and $q = k_q \times n$. Then, we can rewrite (1) as

$$Area = (2 + k_m)(k_p + k_q)P_{nw}^2 n^2 + (2 + k_m)P_{nw}^2 n \,. \quad (2)$$

That is, $Area = O(n^2)$. There are $2np$ crosspoints totally in the p-FETs and n-FETs areas of this crossbar. Unfortunately, not all these $2np$ crosspoints can be utilized as FETs at the same time to implement a logic circuit. Because of the DC voltage drop of the FETs and finite power supply, the number of FETs in each column is limited, which we denote as M. Therefore, the total number of FETs in a crossbar of dimension n is $2Mn$. So far, we conclude that a crossbar of $2Mn$ FETs has an area of $O(n^2)$. Therefore, the transistor density is $O(n^{-1})$, calculated as

$$Transistor\ density = \frac{2M}{(2 + k_m)(k_p + k_q)P_{nw}^2 n + (2 + k_m)P_{nw}^2} \,. \quad (3)$$

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Discussion: The analysis results show that the transistor density of a crossbar logic circuit will decrease when the crossbar dimension increases. Fig 2 shows the relation between transistor density and crossbar dimension n based Equation (3). The solid lines and dashed lines stand for crossbar and MOSFET logic circuits, respectively. Different colors represent different fabrication technologies. It is very clear that the transistor density of a crossbar circuit decreases as the dimension n increases. Another interesting observation is that every two lines with the same color intersect at a point around $n = 25$. In other words, a crossbar circuit has a higher transistor density than its MOSFET counterpart with the same lithography technology when the dimension is less than 25. This shows that the transistor density advantage of crossbar logic circuits over MOSFET logic circuits is achieved because of not only the small nanowire pitch but also the tiny FETs sizes.

2.2 Delay

We analyze first order RC delay of an inverter driving a load capacitor with the same capacitance as a single FET in a crossbar, as shown in Fig 3. In our analysis, we ignore the resistance of horizontal metallic wires because metal, e.g. Cu, has a much higher, typically 100 times, conductivity than silicon. We also ignore the contact resistance between a silicon nanowire and a metallic wire because it is much smaller than the channel resistance [9]. At last, we ignore the capacitance of nanowire, because it can be reduced to a negligible level by using a thick substrate with a low dielectric constant.

Theorem 2: *The delay of a crossbar logic circuit is O(n).*

Proof: In a crossbar of dimension n, as shown in the Fig 3(a), the FETs and contacts are on the x-th and the $(n + y)$-th horizontal wires from the top, respectively. The equivalent circuits during the low-to-high (*LH*) and high-to-low (*HL*) transitions are shown in the Fig 3(b), in which r_{nw} ($r_{nw,p}$ for p-type silicon nanowires and $r_{nw,n}$ for n-type silicon nanowires) is the unit resistance of a silicon nanowire, and R_{on} ($R_{on,p}$ for p-FETs and $R_{on,n}$ for n-FETs) is the channel resistance of a FET. We next calculate the delay for the *LH* transition but the analysis directly applies to the *HL* one too:

$$\tau_{LH} = 0.69C_{fet}(R_{on,p} + (n + y)P_{io} r_{nw,p}) \,; \quad (4)$$

Considering the maximum number of y is n, we have

$$\tau_{LH\max} = 0.69C_{fet}(R_{on,p} + 2nP_{io} r_{nw,p}) \,; \quad (5)$$

As in [10], we denote the intrinsic switching delay of a FET as

$$\tau_{\text{int}} = 0.69C_{fet}R_{on} \,. \quad (6)$$

Then we can rewrite (6) as

$$\tau_{LH\max} = \tau_{\text{int},p}(1 + 2P_{io}\frac{r_{nw,p}}{R_{on,p}}n) \,; \quad (7)$$

Therefore, the delay of a crossbar logic circuit is $O(n)$.

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Discussion: Again, we use parameters from literature to compare the delay of a crossbar inverter with a MOSFET

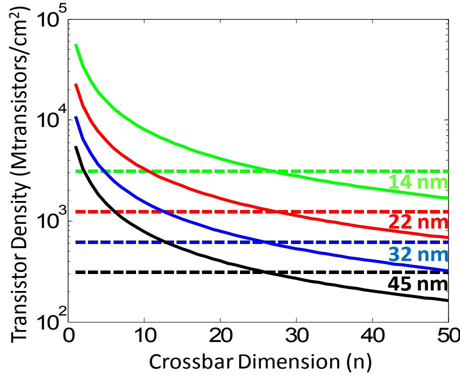

Fig 2: Transistor density versus crossbar dimension: Crossbar (solid); MOSFET (dash).

inverter. Using the parameters of a high performance p-FET [11], we can calculate the delay when $P_{io} = P_{nw} = 45$ nm

$$\tau_{\max} \approx (1+n)\times 1.8 \text{ (ps)}. \quad (8)$$

Since the delay of a 45 nm MOSFET inverter is about 4ps [12], an inverter in a crossbar with $n > 1$ can never outperform MOSFET circuits. According to (7), to reduce the delay, one can limit the dimension, given nanowire technology, reduce the intrinsic switching delay of nanowire FETs, and improve the conductivity of nanowires.

3. Cell-based Design and Integration

Motivated by our reality check, we next introduce a cell design, called *Crossbar Cell*, based on nanowire crossbar arrays with lithographically defined FET crosspoints. Instead of using large crossbars, our solution is to incorporate small crossbars (4 by 4 or smaller) in the form of standard library cells into integrated circuit design. To deal with the fabrication and addressing limitations, our design employs crossbars with nanowires of nanoscale widths but microscale pitches. We present the design, fabrication, and application of the Crossbar Cells next.

3.1 Crossbar Cell Design and Fabrication

Crossbar Cell is based on complementary FET-based nanowire crossbars, as shown in the Fig 4, in which silicon nanowires and metal wires are separated by a low-κ insulator layer. When we put a high-κ insulator layer between a silicon nanowire and a metal wire, the associate crosspoint will be a FET. All the metal wires and insulator layers can be patterned by the standard lithography for MOSFET. The crossbar can be fabricated with MOSFET technology with the only addition of nanoimprinting, which is well developed and ready to incorporate into MOSFET fabrication process [5]. According to the analysis in Section 2, we limit the dimension of the crossbar in a Crossbar Cell.

We next build SPICE models for the Crossbar Cells in Fig 4 and MOSFET cells with identical functions by 45 nm CMOS transistor models from Predictive Technology Model (PTM) [12]. Using SPICE simulation, we obtain the performance of these Crossbar Cells and their MOSFET counterparts and list them in Table I. The Crossbar Cells have much smaller area and capacitance but slightly larger delay than their MOSFET counterparts.

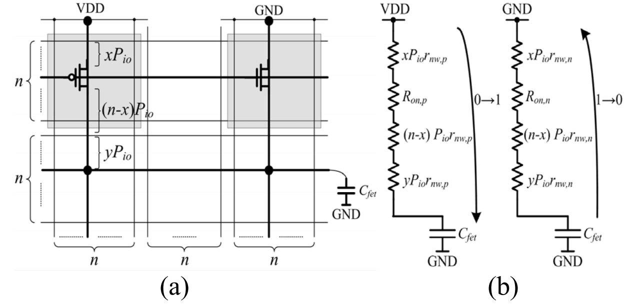

Fig 3: (a) An inverter in a crossbar of dimension *n*; (b) Equivalent circuits for delay analysis.

TABLE I: Parameters for Crossbar and MOSFET cells

Parameters	INV		NAND		NOR	
	MOS FET	Cross bar	MOS FET	Cross bar	MOS FET	Cross bar
Area(μm^2)	0.45	0.05	0.65	0.13	0.65	0.13
Delay (ps)	15.0	18.5	20.2	28.6	26.4	33.5
Cap (fF)	0.74	0.20	0.87	0.30	1.01	0.30

3.2 Integration into Standard Cell-based Design

We use standard benchmark circuits and do logic synthesis to compare the performance, i.e., area, critical path delay, and dynamic power, of these synthesized circuits using different technologies. We chose the largest 20 benchmark circuits from the MCNC91 suite.

Three technology libraries are created. The *MOSFET library* includes seven types of logic gates, or cells, i.e., inverter, NAND and NOR gates with 2, 3, and 4 inputs. The *Crossbar library* is based on 45 nm half-pitch lithography technology, which includes inverter, 2-input NAND and NOR gates. The *M & C library* is the combination of MOSFET and Crossbar libraries. Leveraging the cell selection algorithm provided by Berkeley SIS, we can make tradeoffs between the area, speed, and power.

We perform two sets of synthesis with area and delay minimized, respectively. For dynamic power calculation, we assumed V_{dd} = 1.0 V and the circuits clocked at the maximum speed, i.e., the reciprocal of the critical path delay. The results, as shown in Table II in terms of average over all benchmarks, demonstrate that Crossbar Cells are especially effective in reducing circuit logic area. In the area-optimized case, circuits synthesized with Crossbar and M & C libraries are four times (4X) smaller than their MOSFET counterparts while running only about 10% slower, with all cells being Crossbar Cells. In the delay-optimized case, circuits synthesized with M & C library are

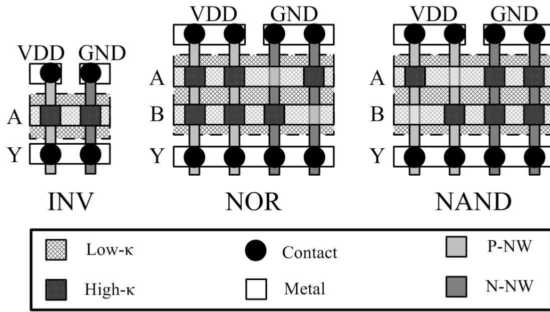

Fig 4: Crossbar Cells with microscale pitch and limited dimension.

about 18% smaller, 9% lower power, and 5% faster than their counterparts in MOSFET. In this case, the Crossbar Cells account for about 30% of all the cells in the synthesized circuits.

TABLE II: Average of synthesized benchmarks

Parameters	Area Minimized			Delay Minimized		
	MOS FET	Cross bar	M&C	MOS FET	Cross bar	M&C
Area (μm^2)	1014.3	247.7	247.7	1160.8	248.6	957.5
Delay (ns)	0.99	1.09	1.09	0.84	1.08	0.80
Power (μW)	695.3	204.8	204.8	802.4	196.9	728.2

By specifying different delay constraints in SIS, we obtain the delay-area tradeoff curves for synthesis with all three libraries, as shown in the Fig 5. The tradeoff curve for M & C library is well below that for MOSFET library, showing that M & C library can significantly reduce the circuit areas (2.5X on average) given the same delay constraint. In contrast, circuits implemented solely with Crossbar Cells (Crossbar library) suffer considerably in the delay-optimized case simply because Crossbar Cells are slower than their MOSFET counterparts. These results highlight that Crossbar Cells must be applied selectively along with MOSFET cells to achieve best design tradeoffs.

4. Conclusions

We analyze the performance of nanowire crossbar-based logic circuit and compared them with their MOSFET counterparts. We show that nanowire crossbars do not scale well in implementing logic and it is more important to have faster nanowire FETs with high channel resistance and low capacitance than fabricating larger arrays of crossbars. Therefore, we propose a Crossbar Cell design based on small nanowire crossbars that can be fabricated with existing nanoimprinting and lithography methods. The design is compatible with the conventional MOSFET fabrication technology and design methodology. We demonstrate that Crossbar Cells can be employed to improve the performance of conventional standard cell-based integrated circuits. Our results with the MCNC91 benchmark suite show that the incorporation of Crossbar Cells into standard MOSFET cells provides a significant reduction in circuit area (4X) and power (3X) at the same lithographical level, with comparable speed, if the circuits are optimized for area. Our results also show that the use of Crossbar Cells improves speed, power, and area simultaneously if optimized for speed.

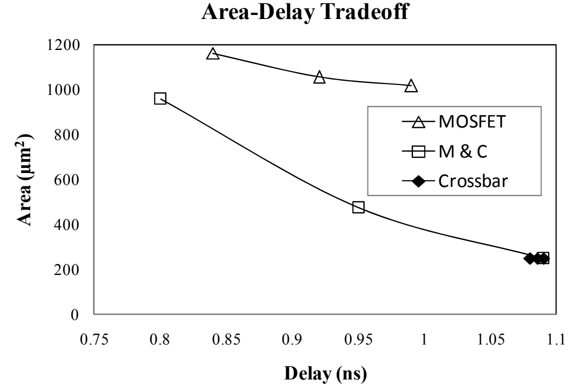

Fig 5: Delay-Area tradeoff.

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