Resistive Switching in Nanogap Systems on SiO_2 Substrates

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Voltage-controlled resistive switching in various gap systems on SiO_2 substrates is reported. The nanoscale-sized gaps are made by several means using different materials including metals, semiconductors, and amorphous carbon. The switching site is further reduced in size by using multiwalled carbon nanotubes and single-walled carbon nanotubes. The switching in all the gap systems shares the same characteristics. This independence of switching on the material compositions of the electrodes, accompanied by observable damage to the SiO_2 substrate at the gap region, bespeaks the intrinsic switching from post-breakdown SiO_2. It calls for caution when studying resistive switching in nanosystems on oxide substrates, since oxide breakdown extrinsic to the nanosystem can mimic resistive switching. Meanwhile, the high ON/OFF ratio ($\approx 10^5$), fast switching time (2 μs, tested limit), and durable cycles show promising memory properties. The observed intermediate states reveal the filamentary nature of the switching.

Keywords:
- carbon nanotubes
- nanogaps
- nonvolatile memory
- resistive switching
- SiO_2

1. Introduction

Resistive switching in various materials such as metal oxides,[1,2] chalcogenides,[3] and organic materials[4–6] has been intensively studied as a candidate for future nonvolatile memory.[7] Recently, resistive switching has been extended to new quasi-1D and 2D materials such as encapsulated nanowires,[8] multiwalled carbon nanotubes (MWCNTs),[9] and graphene sheets.[10] In these nanostructures, the constriction in at least one dimension facilitates the observation of the switching events. The direct observations of nanoscale-sized gap or void structures in these systems suggest switching mechanisms based on the electrically driven close-and-break motion of the material at the gap/void region. Less attention has been paid to the SiO_2 substrate material due to its generally good dielectric (insulating) properties. It has been shown that the amorphous form of SiO[11–16] or a defective SiO_x ($x < 2$) surface[17] can exhibit memory phenomena, in which structural defects induced by high local fields are among the proposed causes.[11] For a gap system at the nanoscale, or a nanogap system, it is expected that a high local field is built up during the switching between high-impedance (OFF) and low-impedance (ON) states. It is therefore of great interest to investigate local field effects on the commonly used SiO_2 substrate material. We demonstrate resistive switching phenomena in various nanogap systems made by different materials and means on SiO_2 substrates. The similar switching characteristics in all the systems point to the most likely cause: SiO_2 breakdown (BD)-induced filaments, possibly through direct Si–Si bond formation.

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2. Results and Discussion

Shown in Figure 1a is an initial gap system in a pair of W electrodes separated by ≈50 nm on a thermal-oxidized Si surface (the SiO_2 thickness is 200 nm and the same thickness is used for all the following devices), defined by a standard electron-beam lithography (EBL) and lift-off process. Electrical characterizations were performed using an Agilent 4155C semiconductor parameter analyzer and a data acquisition system (NI USB-6251 BNC) in a vacuum environment (≈10^{-5} Torr). The Si substrate was kept floating (i.e., sitting on a glass substrate) during the measurements and is the same for all the measurements performed on other devices in this study. Bias voltage was applied between the two electrodes by sweeping from 0 to 30 V and then back to 0 V (Figure 1b). The device shows no conduction during the initial forward sweep from 0 to 25 V (e.g., the current is at the noise level, ≈10^{-12} A, of the instrument). Substantial conduction begins at ≈25 V with a sudden current increase at ≈30 V, indicating a SiO_2 BD. An irreversible resistance change takes place in the post-BD device, indicated by the increased current level during the subsequent backward sweep from 30 to ≈6 V. The sudden current (or conductance) rise at ≈6 V (indicated by the small black arrow in Figure 1b) in this backward sweep indicates the initiation of hysteretic current–voltage curves (*I–V*s) essential for memory switching. Figure 1c shows the two characteristic *I–V*s of the post-BD device: in a forward sweep (0 V → 10 V, grey curve) beginning with an OFF state,[18] the device jumps to an ON state at ≈3.5 V and goes back to OFF at ≈5 V. In the backward sweep (10 V → 0 V, black curve), it jumps from an OFF state to an ON state at ≈5 V and keeps the ON state below 5 V. Consequently, a current hysteresis is produced in the bias range below 3.5 V (region **I** in Figure 1c). The underlying information about the two *I–V*s is that a fast voltage drop edge above 3.5 V (region **II** in Figure 1c) can set the conductance of the device into a value corresponding to the set voltage.[11] For example, a +4 V (2 μs, instrumentation limit) pulse "writes" the device into an ON state, while a +10 V pulse "erases" the device to an OFF state. The set states can be read out in the lower bias region **I** without being destroyed, demonstrating the nondestructive memory property. Figure 1d shows the corresponding memory cycles in the device, with an ON/OFF ratio close to 10^5.

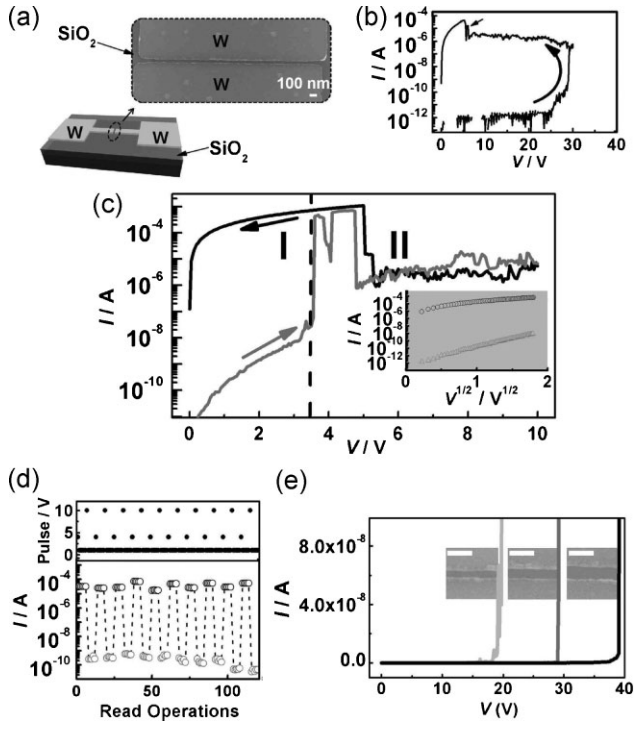

Figure 1. a) Schematic of the W–W gap and the SEM image. b) *I–V* of the initial sweep from 0 V → 30 V → 0 V in the as-made 50-nm-gap device. c) *I–V*s of a forward (0 V → 10 V, grey curve) and subsequent backward (10 V → 0 V, black curve) in the electroformed device. The black dashed vertical line separates region **I** (reading) and region **II** (writing/erasing). The inset shows the *I–V*s in region **I** using an $I–V^{1/2}$ plot. d) Memory cycles of the device: after every five readings at +1 V, the device was set by an erasing pulse +10 V or a writing pulse +4 V. The top panel shows the corresponding pulses. e) *I–V*s in three as-made devices with W–W spacing of 30 (light grey curve), 50 (grey curve), and 70 nm (black curve). The pictures beside each curve show the corresponding SEM images of the devices, with the white scale bars 100 nm in length.

The SiO_2 BD-induced conduction is supported by the linear dependence of BD threshold voltage on the electrode–electrode spacing. Gap spacing of ≈30, ≈50, and ≈70 nm result in BD threshold values of ≈18, ≈29, and ≈39 V, respectively (Figure 1e). The corresponding averaged electric field is ≈6 MV cm^{-1}, which falls into the typical BD values of SiO_2.[19] The surface region is also expected to induce BD more easily than bulk given the higher likely density of defects. The sudden current increase during the first sweep is accompanied by observable SiO_2 substrate damage in the gap region. Subsequent forward or backward sweeps usually undergo gradual current increases and fluctuations having the characteristics increasingly like those of the forward or backward *I–V*s depicted in Figure 1c. This electroforming process resembles that observed in vertical M/SiO/M (M denotes conducting electrodes) switching systems,[11] in which the amorphous form of SiO is the conducting and switching medium. The non-ohmic *I–V*s, both for ON and OFF states, are dominated by Poole–Frenkel conduction having the characteristic of $\log(I) \propto V^{1/2}$ (inset in Figure 1c). The calculated[20] Poole–Frenkel field-lowering coefficient ($\beta_{PF} = 3.4 \times 10^{-5}$ eV $m^{1/2}V^{-1/2}$) from the OFF state is very close to the theoretical one of $\beta_{PF} = 3.8 \times 10^{-5}$ eV $m^{1/2}V^{-1/2}$ and other experimental values in SiO_x.[21]

The electric-field-assisted BD in conducting materials[10,22,23] offers another means for gap generation. A lift-off process was used to define an amorphous carbon (α-C) stripe (≈40-nm thick, by sputtering from a carbon graphite target) on a SiO_2 substrate. Two Pt electrodes with a comparatively large spacing (≈0.8 μm) were then defined (see top inset in Figure 2a). A 5-min annealing at 600 °C in an Ar/H_2 environment was performed to improve the conductivities of both the α-C layer and contacts. Bias voltage was applied between the two electrodes. The sudden current drop at ≈5.8 V (Figure 2a) indicates a BD in the α-C stripe. A scanning electron microscopy (SEM) image reveals a cracked region perpendicular to the current direction in the α-C stripe (Figure 2b). The reduced conduction immediately after the α-C BD (see the subsequent backward sweep in bottom inset in

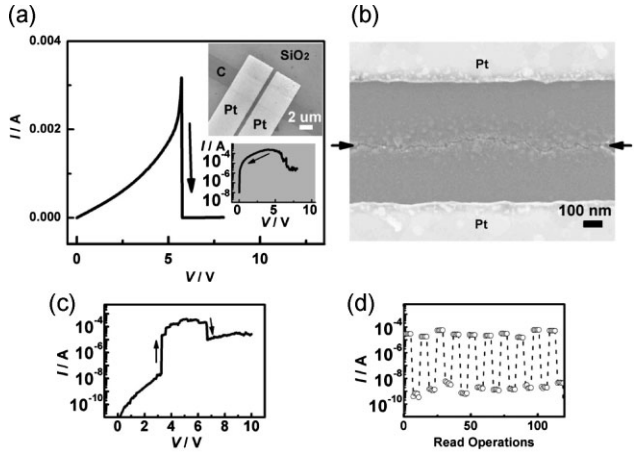

Figure 2. a) *I–V* of the initial forward sweep in the as-made α-C device. The top inset shows the SEM image of a patterned device. The bottom inset shows the *I–V* of the subsequent backward sweep right after α-C BD. b) SEM image of the α-C stripe between the two Pt electrodes after the α-C BD. The black arrows indicate the BD-induced gap region. c) The characteristic forward *I–V* in the electroformed device. d) Memory cycles using +1 V (5 reads), +4 V (write), and +10 V (erase) pulses.

Figure 2a) has a similar Poole–Frenkel feature to that seen in Figure 1c, indicating the disruption of the α-C layer and simultaneous BD in SiO_2 in the gap region. The conductance jump at ≈6 V (bottom inset in Figure 2a) during this backward sweep initiates the similar electroforming process as discussed above in the W–W gap (Figure 1b). The characteristic forward *I–V* (Figure 2c) and switching (Figure 2d) show similar features to those in the W–W gap (Figure 1c and d) such as current levels, writing/erasing voltages, ON/OFF ratio, and switching times (2 μs, tested limit). While the threshold BD voltage in α-C tends to be proportional to the electrode–electrode spacing, the writing/erasing voltages for switching tend to be independent of it, consistent with the local switching nature within the gap region; since the collective resistance of the contacts and the α-C layer is considerably smaller than that of the gap region, the bias voltage drops largely across the gap.

Compared to the EBL-defined W–W gaps, the α-C BD-induced gap reduces the initial BD and electroforming voltage of SiO_2 in the gap region since the narrowest part is expected to be smaller than 30 nm. On the other hand, it also offers a better way to investigate the details of the gap region by removing the α-C layer without destruction to the SiO_2 substrate. α-C was removed by oxidation (750 °C in air) in the same switching device. SEM images show substantial damage to the SiO_2 part corresponding to the gap region. Further control tests were performed in devices with same α-C thicknesses and electrode spacings to investigate how the damage to SiO_2 forms. In one group, we produced BD in the α-C layer by one single sweep to a voltage above the α-C BD threshold value, while in the other we performed multiple sweeps up to a voltage slightly below the α-C BD threshold value (thus no gap generation). After the α-C removal, observable damage to the SiO_2 substrate at the gap region in the first group was found, but no damage to the SiO_2 substrate was found in the second group. The results reveal that i) the gap generation in the α-C layer simultaneously induces SiO_2 BD within the gap region, which is consistent with the reduced conduction (through post-BD SiO_2) having the Poole–Frenkel feature right after the α-C BD discussed above; 2) the damage to SiO_2 is mainly through local electric-field induced BD, as opposed to local heating, since a great reduction in current local heating is expected after the disruption of α-C layer in the gap region due to the sudden current drop. We also found that extended electroforming process and switching cycles tend to have more pronounced damage to SiO_2 substrate in the gap region. These results indicate the role of SiO_2 in switching in the gap region.

The post-BD SiO_2 switching nature is further emphasized by using a different material as the gap-generation medium. Electrical BD in a titanium nitride (TiN) stripe on a SiO_2 substrate leads to similar gap structure and switching (see Supporting Information, S1). Compared to that in α-C stripe, the gap in a TiN stripe is usually located at the TiN–electrode interface instead of between the electrodes. The possible reason is that the Schottky barrier at the TiN–electrode interface (since TiN is semiconducting) enhances the local field and facilitates the TiN BD at that location, as opposed to an efficient C–Pt electrical contact in the α-C stripe, where C BD is likely to happen at the least heat-dissipation region far away from both electrodes.

A gap due to electric-field BD is less likely to form in metal stripes because the high current density usually melts the metal before a BD and the surface tension of liquid metal tends to form droplets, preventing a narrow and well-aligned gap. However, a thin metal film tends to form discrete islands[24] and nanogaps may form naturally between individual islands. For this purpose, an Al thin film (≈10-nm-thick) was deposited by sputtering on SiO_2 between two Pt electrodes. The surface morphology of the deposited Al studied by atomic force microscopy (AFM) shows discontinuous granular features (Figure 3a). A voltage sweep was applied between the two electrodes for the as-made device. Unlike that in α-C or TiN stripes, the initial forward sweep (0 V → 20 V) shows a much lower conductance and no sudden current drop (Figure 3b). This further indicates the discontinuity of the Al film. The subsequent backward sweep (20 V → 0 V), with a conductance jump, indicates the initiation of hysteretic behavior. The SEM image of the electroformed device shows a granular Al surface between the electrodes (Figure 3c) with no such apparent gap (Figure 3d) as that produced by BD in α-C or TiN stripes, which is consistent with the *I–V* feature of the initial sweep discussed and in support of the idea of switching in as-formed island–island gaps. Although the actual switching site is unknown due to numerous indistinguishable gaps between islands, it is expected that the relatively high resistance of the Al film reduces both the current and effective voltage drop across the switching site. Therefore, the switching device has higher writing/erasing voltages (Figure 3e) and lower ON current (Figure 3f).

From the device perspective, one interesting question is, How small can the device become? Furthermore, a small and constricted switching size may offer a clearer view of the switching location, while it is relatively difficult to distinguish the actual switching site in a wide α-C stripe, for example, whether the switching happens uniformly along the entire gap

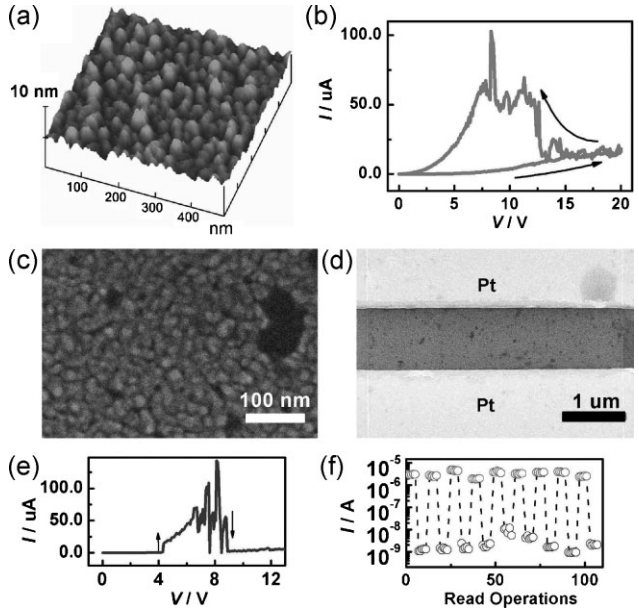

Figure 3. a) AFM surface morphology of Al film between the two Pt electrodes. b) *I–V* of the initial double sweep (0 V → 20 V → 0 V, indicated by the black arrows) in the as-made Al island device. c) SEM image of the Al film of the switching device, showing the granular structures. d) SEM image of the Al island after switching, showing no apparent gap structure. e) The characteristic *I–V* of a forward sweep in the electroformed Al island device. f) Memory cycles using +1 V (5 reads), +6 V (write), and +14 V (erase) pulses.

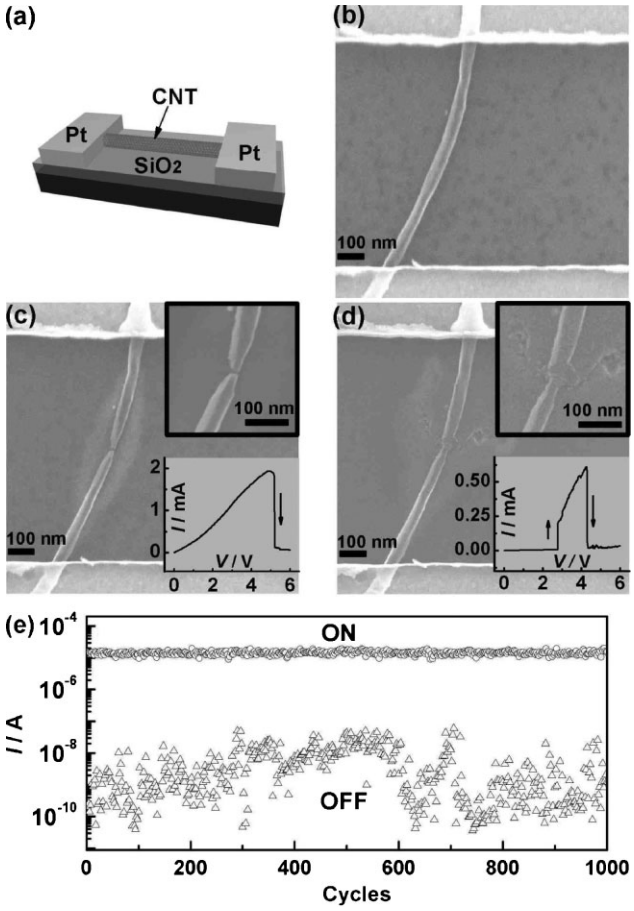

Figure 4. a) Schematic of two Pt electrodes patterned on a MWCNT atop a SiO_2 substrate. b) SEM image of the as-made MWCNT device before electrical characterization. c) SEM image of the same MWCNT immediately after BD. The bottom inset shows the BD *I–V* and the top inset is a magnified view showing the gap structure at the BD region. d) SEM image of the same MWCNT device after electroforming. The bottom inset shows the corresponding characteristic forward *I–V* and the top inset is the magnified view of the gap region showing SiO_2 damage. e) 10^3 cycles in a second MWCNT device, with the reading, writing, and erasing pulses of +0.5 V, +3.5 V, and +6 V, respectively.

region or locally. The electrical BD in MWCNTs[25] provides a potential means for further reduction in gap size. For this purpose, two Pt electrodes were patterned on the ends of a MWCNT[26] (Mitsui & Co., Ltd.) with a diameter ≈60 nm (Figure 4a). Figure 4b shows the SEM image of the pristine device. Electrical BD begins at a voltage of ≈5 V indicated by a sudden current drop (bottom inset in Figure 4c). The corresponding SEM image right after this BD shows a broken gap region (Figure 4c and top inset). The subsequent sweeps electroform the device, showing the characteristic switching *I–V* (bottom inset in Figure 4d) similar to those observed in all the above devices. The SEM image of the electroformed device shows clear damage to the SiO_2 at the gap region, extending beyond the nanotube (Figure 4d and top inset). Note that switching in electrical BD MWCNTs was reported previously.[9] The ON and OFF states were achieved by close-and-break motion of the carbon nanotube shells from the two broken ends, and were stable up to only several cycles.[9] The switching here is attributed to the post-BD SiO_2 at the gap region and is stable with extended cycling (Figure 4e). The non-mechanical switching of the nanotube itself is also supported by the high yield in our devices (e.g., ten out of ten MWCNT devices tested show similar switching) regardless of the actual details of the broken ends. This is in contrast to nanotube-based mechanical switching since we expect that both the broken gap size and the morphology of the broken ends would affect the behavior.

Single-walled carbon nanotubes (SWCNTs) are candidates for ultra-small constrictions. Electrical BD in metallic SWCNTs was reported and used as a means for sorting semiconducting SWCNTs.[27] Ti/Pt electrodes were patterned on a metallic SWCNT with a diameter of ≈2 nm. Electrical BD takes place at ≈8.5 V (Figure 5a). Figure 5b and c shows the characteristic *I–V* and switching after BD and electroforming. The AFM image of the electroformed device shows the broken region in the SWCNT (Figure 5d). The corresponding SEM image in Figure 5e shows a dark dot at the gap region, indicating hole-like damage to the SiO_2 substrate, which is also inferred from the AFM image. The comparatively small ON current (Figure 5c) in the SWCNT device is mainly attributed to the contact resistance between the broken nanotube ends and the post-BD SiO_2 in the gap region, as a good electric contact to metallic SWCNTs with diameters below 2 nm usually requires specific metals.[28] This contact resistance also reduces the effective voltage drop across the gap, resulting in higher writing/erasing voltages (Figure 5b). The SWCNT device retains the switching behavior at an elevated temperature of 100 °C at

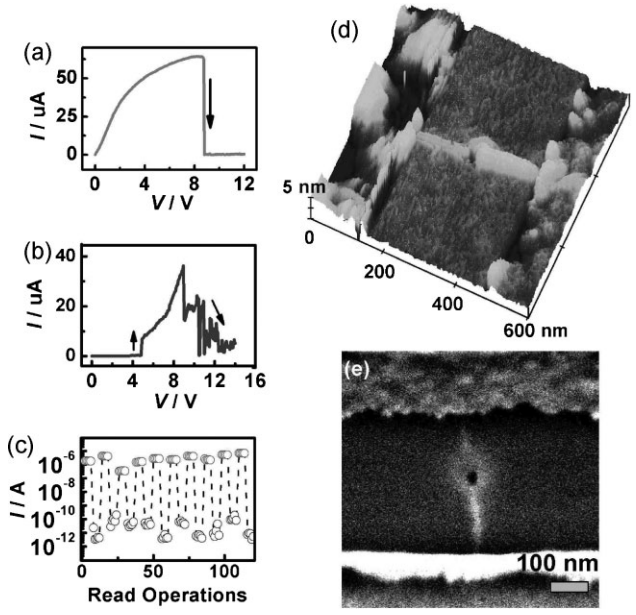

Figure 5. a) The initial BD *I–V* of the SWCNT device. b) The characteristic forward *I–V* in the electroformed device. c) Memory cycles using +2 V (5 reads), +8 V (write), and +14 V (erase) pulses. d) AFM image of the electroformed SWCNT device. e) Corresponding SEM image of the same electroformed SWCNT device.

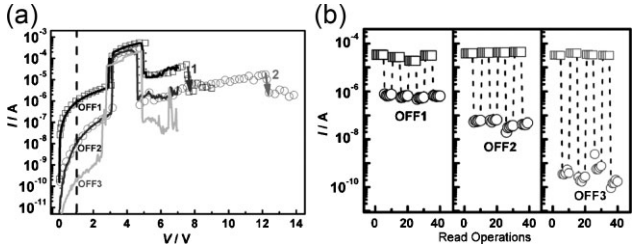

Figure 6. a) *I–V* evolutions in an electroformed MWCNT device. Starting from a forward *I–V* with an initially established "OFF1" state (0 V → 7 V, black curve), the subsequent forward sweep (grey curve, squares) up to a higher voltage (0 V → 9 V) lowers the OFF state (grey arrow 1 at ≈7.5 V). A new characteristic forward *I–V* with a lower initial conduction state "OFF2" is established subsequently (dark grey curve). By sweeping to an even higher voltage of 14 V (grey curve, circles), a second conductance reduction in the OFF state is initiated (grey arrow 2 at ≈12 V). Similarly, a third characteristic *I–V* featuring an even lower initial conduction state "OFF3" establishes thereafter (light grey curve). b) Memory cycles using the same set of +1 V (5 reads), +3.5 V (write), and +7 V (erase) pulses in the same device, with the left, middle, and right columns corresponding to the established black ("OFF1"), dark grey ("OFF2"), and light grey ("OFF3") characteristic *I–V* curves in (a).

10^{-5} torr, which excludes adsorption of water as the cause for the observed effect.

All the above devices share the similarities once operational. These include similar writing/erasing voltages and currents (the reduced ON currents and increased writing/erasing voltages in Al island and SWCNT devices are due to high film or contact resistances), switching times, and noise distributions. The comparatively large current fluctuation in the erasing bias region observed in all the devices is another characteristic of SiO_x conduction.[11] The approximate independence of switching on the (effective) electrode materials ranging from metals (W, Al), conducting nonmetal (C), semiconductor (TiN), to carbon nanotubes, along with the electroforming processes and observable damage to the SiO_2 substrate in the gap regions, bespeaks the intrinsic post-BD SiO_2 switching nature. This is confirmed by making similar α-C stripe structures on Si_3N_4 substrates, in which switching was not observed after the gap generation; severe substrate damage is usually observed in the gap region following an electroforming attempt.

Common features observed in all the above devices are the various intermediate conduction states. As shown in Figure 6a for an initially established MWCNT-based device, a characteristic forward (0 V → 7 V) *I–V* (black curve, "OFF1"), an OFF state with a current level of $\approx 10^{-6}$ A can be set by a +7 V pulse (see cycles in the left column in Figure 6b). By sweeping to a higher voltage of 9 V (grey curve, squares), a lower conduction state appears, indicated by a sudden current drop at ≈7.5 V (grey arrow 1). In the subsequent sweep, a new *I–V* featuring a lower OFF state is established (dark grey curve, "OFF2"), and the same +7 V pulse now sets the OFF state to a current level of $\approx 10^{-8}$ A (cycles in the middle column in Figure 6b). The OFF current can be further reduced by sweeping to an even higher voltage of 14 V (grey curve, circles) during which a second conduction reduction appears at ≈12 V (grey arrow 2). This leads to a third *I–V* (light grey curve, "OFF3") with an OFF current level of $\approx 10^{-10}$ A that can be set by the same erasing pulse of +7 V (cycles in the right column in Figure 6b). Multiple intermediate conduction states are an indication of filamentary conduction in oxides,[29] in which different states can be viewed as formation/termination of new/existing percolation paths.[29,30] To an extent, the current fluctuations in the erasing region (light grey curve, "OFF3" in Figure 6a) can be viewed as various metastable states, for example, same erasing voltages can produce different OFF currents if they encounter current fluctuations of different magnitudes. This is well-reflected in the 10^3 cycles of the MWCNT device, in which the OFF states undergo various conductance states (Figure 4e). We attribute this to be the main cause of instability in the current device performance.

3. Conclusions

In summary, we have demonstrated reproducible memory switching in various nanogap systems on SiO_2 substrates. The lack of dependence of the switching behaviors on electrode materials points to a common mechanism, post-BD SiO_2 switching in the gap region. It is therefore important to exercise caution when building resistive switching nanosystems on SiO_2 substrates. Efforts should be taken to distinguish the switching cause. The high ON/OFF ratio, fast switching time, and durable cycles demonstrated here show interesting memory properties. In particular, the small switching site demonstrated in a SWCNT shows the feasibility of high-density SiO_2-based memory arrays if a vertical embodiment could be realized. The observed intermediate states reveal the filamentary conduction

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nature in post-BD SiO_2 switching that is likely Si–Si wire formation, although a further investigation of the individual filamentary path is needed. The post-BD SiO_2 conduction suggests a possible mechanistic scenario for the switching that was observed in graphitic memories.[23,31]

4. Experimental Section

Materials: Amorphous carbon film, TiN film, Al metal islands, and Pt/W electrodes were deposited by sputtering using a CrC-150 Sputtering System (TORR International Inc.) with a base pressure 5.0×10^{-5} Torr. SWCNTs were grown on SiO_2/Si by chemical vapor deposition using Fe/Mo catalyst at 975 °C with CH_4 flow 2 sccm and H_2 flow 4 sccm (more details can be found in Reference [32]). MWCNTs (Mitsui & Co., Ltd.) were dispersed on SiO_2/Si substrate by spin-coating method.

Characterization: SEM images and EBL were performed on a JSM-6500F SEM system (JEOL Ltd.). An ambient AFM system was also used for surface imaging in the SWCNT device and the Al film. Electrical characterization was performed using an Agilent 4155C semiconductor parameter analyzer and a data acquisition system (NI USB-6251 BNC) in a vacuum environment ($\approx 10^{-5}$ Torr).

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[1] K. Szot, W. Speier, G. Bihlmayer, R. Waser, *Nat. Mater.* **2006**, *5*, 312–320.
[2] J. J. Yang, M. D. Pickett, X. Li, D. A. A. Ohlberg, D. R. Stewart, R. S. Williams, *Nat. Nanotechnol.* **2008**, *3*, 429–433.
[3] Y. Hirose, H. Hirose, *J. Appl. Phys.* **1976**, *47*, 2767–2772.
[4] J. Y. Ouyang, C. W. Chu, C. R. Szmanda, L. P. Ma, Y. Yang, *Nat. Mater.* **2004**, *3*, 918–922.
[5] R. C. Scott, L. D. Bozano, *Adv. Mater.* **2007**, *19*, 1452–1463.
[6] R. T. Weitz, A. Walter, R. Engl, R. Sezi, C. Dehm, *Nano Lett.* **2006**, *6*, 2810–2813.
[7] R. Waser, M. Aono, *Nat. Mater.* **2007**, *6*, 833–840.
[8] S. Meister, D. T. Schoen, M. A. Topinka, A. M. Minor, Y. Cui, *Nano Lett.* **2008**, *8*, 4562–4567.
[9] V. V. Deshpande, H.-Y. Chiu, H. W. Ch, Postma, C. Miko, L. Forro, M. Bockrath, *Nano Lett.* **2006**, *6*, 1092–1095.
[10] B. Standley, W. Bao, H. Zhang, J. Bruck, C. N. Lau, M. Bockrath, *Nano Lett.* **2008**, *8*, 3345–3349.
[11] G. Dearnaley, A. M. Stoneham, D. V. Morgan, *Rep. Prog. Phys.* **1970**, *33*, 1129–1191.
[12] J. G. Simmons, R. R. Verderber, *Proc. R. Soc. A.* **1967**, *301*, 77–102.
[13] G. Dearnaley, D. V. Morgan, A. M. Stoneham, *J. Non-Cryst. Solids* **1970**, *4*, 593–612.
[14] G. Dearnaley, *Thin Solid Films* **1969**, *3*, 161–174.
[15] R. E. Thurstans, P. C. Wild, D. P. Oxlety, *Thin Solid Films* **1974**, *20*, 281–286.
[16] M. Shatzkes, M. Av-Ron, R. M. Anderson, *J. Appl. Phys.* **1974**, *45*, 2065–2077.
[17] J. Yao, L. Zhong, D. Netelson, J. M. Tour, *Appl. Phys. Lett.* **2008**, *93*, 253101.
[18] A fast voltage drop edge is expected at the end of each forward sweep, which sets the device state.[11] So the beginning conduction state for a forward sweep is determined by the previous forward sweep. Here the characteristic forward *I–V* was obtained after at least another forward sweep prior to it in the same voltage range. So it begins with an OFF state. All the following characteristic forward *I–V*s were obtained in this way, unless otherwise specified.
[19] Y. Satoh, Y. Murakami, H. Furuya, T. Shingyouji, *Appl. Phys. Lett.* **1994**, *64*, 303–305.
[20] The Poole–Frenkel expression[21] is $I = I_0 \exp\left(\frac{\beta_{PF} E^{1/2}}{kT}\right)$ (1) where k is the Boltzmann constant, T the temperature, and E the electric field. We used room temperature (300 K) and a gap width $d = 50$ nm ($E = V/d$) for fitting.
[21] R. D. Gould, M. G. Lopez, *Thin Solid Films* **2003**, *433*, 315–320.
[22] Y. Naitoh, Y. Morita, M. Horikawa, H. Suga, T. Shimizu, *Appl. Phys. Express* **2008**, *1*, 103001.
[23] Y. Li, A. Sinitskii, J. M. Tour, *Nat. Mater.* **2008**, *7*, 966–971.
[24] A. Wokaun, J. G. Bergman, J. P. Heritage, A. M. Glass, P. F. Liao, D. H. Olson, *Phys. Rev. B* **1981**, *24*, 849–856.
[25] P. G. Collins, M. Hersam, M. Arnold, R. Martel, P. Avouris, *Phys. Rev. Lett.* **2001**, *86*, 3128–3131.
[26] M. Endo, *Chem. Tech.* **1988**, *18*, 568–576.
[27] P. G. Collins, M. S. Arnold, P. Avouris, *Science* **2001**, *292*, 706–709.
[28] W. Kim, A. Javey, R. Tu, J. Cao, Q. Wang, H. Dai, *Appl. Phys. Lett.* **2005**, *87*, 173101.
[29] D. C. Kim, S. Seo, S. E. Ahn, D.-S. Suh, M. J. Lee, B.-H. Park, I. K. Yoo, I. G. Baek, H.-J. Kim, E. K. Yim, J. E. Lee, S. O. Park, H. S. Kim, U-In Chung, J. T. Moon, B. I. Ryu, *Appl. Phys. Lett.* **2006**, *88*, 202102.
[30] T. P. Chen, M. S. Tse, X. Zeng, *Appl. Phys. Lett.* **2001**, *78*, 492–494.
[31] A. Sinitskii, J. M. Tour, *ACS Nano*, DOI: 10.1021/nn9006225.
[32] Z. Jin, H. Chu, J. Wang, J. Hong, W. Tan, Y. Li, *Nano Lett.* **2007**, *7*, 2073–2079.

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